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L7	2	l4 and ((retirement near2 (payload adj2 array))same ((shift$3 or mov$3 or position or location or advanc$3)with (read adj pointer)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 14:59
L8	2	l4 and (((retirement near2 (payload adj2 array))same ((shift$3 or mov$3 or position or location or advanc$3)with (read adj pointer))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 14:59

L9	2	I5 and (((retirement near2 (payload adj2 array))same ((shift$3 or mov$3 or position or location or advanc$3)with (read adj pointer))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 14:58
L10	1	I6 and (((retirement near2 (payload adj2 array))same ((shift$3 or mov$3 or position or location or advanc$3)with (read adj pointer))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 14:58
L11	0	(((reorder$3 orretirement) near2 (payload adj2 (buffer or array)))same ((shift$3 or mov$3 or position or location or advanc$3)with (read adj pointer)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 15:00
L12	5	(((reorder$3 or retirement) near2 (payload adj2 (buffer or array)))same ((shift$3 or mov$3 or position or location or advanc$3)with (read adj pointer)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 15:02
L13	5	(((reorder$3 or retirement) near2 (payload adj2 (buffer or array)))and ((shift$3 or mov$3 or position or location or advanc$3)with (read adj pointer)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 15:02

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1 Mondrian memory protection

Emmett Witchel, Josh Cates, Krste Asanović

October 2002 **Proceedings of the 10th international conference on Architectural support for programming languages and operating systems**, Volume 37 , 30 , 36 Issue 10 , 5 , 5

Full text available: 📄 pdf(1.53 MB)   Additional Information: full citation, abstract, references, citings

Mondrian memory protection (MMP) is a fine-grained protection scheme that allows multiple protection domains to flexibly share memory and export protected services. In contrast to earlier page-based systems, MMP allows arbitrary permissions control at the granularity of individual words. We use a compressed permissions table to reduce space overheads and employ two levels of permissions caching to reduce run-time overheads. The protection tables in our implementation add less than 9% overhead to ...

2 Superscalar architectures: Select-free instruction scheduling logic

Mary D. Brown, Jared Stark, Yale N. Patt

December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**

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Pipelining allows processors to exploit parallelism. Unfortunately, critical loops---pieces of logic that must evaluate in a single cycle to meet IPC (Instructions Per Cycle) goals--- prevent deeper pipelining. In today's processors, one of these loops is the instruction scheduling (wakeup and select) logic [10]. This paper describes a technique that pipelines this loop by breaking it into two smaller loops: a critical, single-cycle loop for wakeup; and a non-critical, potentially multi-cycle, lo ...

3 Spinach: a liberty-based simulator for programmable network interface architectures

Paul Willmann, Michael Brogioli, Vijay S. Pai

June 2004 **ACM SIGPLAN Notices , Proceedings of the 2004 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools for embedded systems**, Volume 39 Issue 7

Full text available: 📄 pdf(336.99 KB)   Additional Information: full citation, abstract, references, citings, index terms

This paper presents Spinach, a new simulator toolset specifically designed to target programmable network interface architectures. Spinach models both system components that are common to all programmable environments (e.g., ALUs, control and data paths, registers, instruction processing) and components that are specific to the embedded systems and network interface environments (e.g., software-controlled scratchpad memory, hardware assists for DMA and medium access control).Spinach is built on ...

Keywords: embedded systems, programmable network interfaces, simulation

4 Co-design and synthesis: An efficient system-on-a-chip design methodology for networking applications
Valentina Salapura, Christos J. Georgiou, Indira Nair
September 2004 **Proceedings of the 2004 international conference on Compilers, architecture, and synthesis for embedded systems**
Full text available: pdf(184.23 KB)   Additional Information: full citation, abstract, references, index terms

This paper presents a System-on-a-Chip design methodology that uses a microprocessor subsystem as a building block for the development of chips for networking applications. The microprocessor subsystem is a self-contained macro that functions as an accelerator for computation-intensive pieces of the application code, and complements the standard components of the SoC. It consists of processor cores, memory banks, and well-defined interfaces that are interconnected via a high-performance switch. ...

Keywords: network processor, system-on-a-chip

5 Commercially viable active networking
Stuart Eichert, Osman N. Ertugay, Dan Nessett, Suresh Vobbilisetty
January 2002 **ACM SIGOPS Operating Systems Review**, Volume 36 Issue 1
Full text available: pdf(1.52 MB)   Additional Information: full citation, abstract, references, citings, index terms

Active Networking is a new technology receiving significant attention from the research community. To this point, however, it has not been examined from the perspective of commercial viability. This paper presents an analysis of active networking issues with a view to its possible uses in a commercial environment. It then describes a prototype system built to address these issues.

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1 Image and video databases: Image retrieval with embedded region relationships   ▬
Sharat Chandran, Naga Kiran
March 2003 **Proceedings of the 2003 ACM symposium on Applied computing**

Full text available: 📄 pdf(1.77 MB)   Additional Information: full citation, abstract, references

Image retrieval based on content from digital libraries, multimedia databases, the Internet, and other sources has been an important problem addressed by several researchers. In this regard, one cannot overestimate the use of appropriate features such as color, texture, and shape. It has also become increasingly evident that the decomposition of images into regions is critical for useful results.In this paper we further study region-based image retrieval. We argue that a relationship between reg ...

Keywords: database, multimedia, region, similarity, subgraph

2 Report on the workshop on design & performance issues in parallel architectures   ▬
Satish K Tripathi, Steve Kaisler, Sharat Chandran, Ashok K Agrawala
January 1987 **ACM SIGMETRICS Performance Evaluation Review**, Volume 14 Issue 3-4

Full text available: 📄 pdf(679.42 KB)   Additional Information: full citation, abstract, citings, index terms

Machines that perform computations in parallel have come into vogue today partly prodded by technology and user needs. In the early spring of '86, a workshop was held under the auspices of the University of Maryland Institute for Advanced Computer Studies (UMIACS) to investigate the design and the notusually-addressed issue of the performance of these machines. This report serves as a record of the workshop though it does not promise to be a transcript of the various sessions. About a dozen pres ...

3 A selective repeat ARQ scheme for point-to-multipoint communications and its throughput analysis   ▬
S R Chandran
August 1986 **ACM SIGCOMM Computer Communication Review , Proceedings of the ACM SIGCOMM conference on Communications architectures & protocols**, Volume 16 Issue 3

Full text available: 📄 pdf(929.24 KB)   Additional Information: full citation, abstract, references, citings, index terms

Selective repeat automatic-repeat-request (ARQ) schemes with finite receiver buffer have been studied and analyzed extensively for point-to-point communications. In this paper, we propose a selective repeat ARQ scheme for point-to-multipoint communications where each receiver has a finite buffer size. A lower bound on the throughput efficiency of the proposed scheme is obtained. Computation of the lower bound and simulation of the scheme reveal that the ARQ scheme performs quite satisfactor ...

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Chandran, A.P.; Najafi, K.; Wise, K.D.;
[Engineering in Medicine and Biology, 1999. 21st Annual Conf. and the 1999 Annual Fall Meeting of the Biomedical Engineering Soc.] BMES/EMBS Conference, 1999. Proceedings of the First Joint
Volume 1, 13-16 Oct. 1999 Page(s):386 vol.1
Digital Object Identifier 10.1109/IEMBS.1999.802463

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